MASKING STRUCTURE HAVING MULTIPLE LAYERS INCLUDING AN AMORPHOUS CARBON LAYER

Related Applications

This application is related to the following co-pending and commonly assigned application; attorney docket number 303.864US1, application serial number _____, entitled "TRANSPARENT AMORPHOUS CARBON STRUCTURE SEMICONDUCTOR DEVICES" which is hereby incorporated by reference.

Field of Invention

The present invention relates generally to semiconductor devices, more particularly to masking structures in the semiconductor devices.

Background

Semiconductor devices such as memory devices reside in many computers and electronic products to store data. A typical semiconductor device has many layers of different materials formed on a semiconductor wafer.

During manufacturing, the layers go through many processes. For example, a patterning process puts patterns on the layers. Some patterning processes use a mask to transfer patterns from the mask to the layers underneath the mask. The patterns on the mask itself are often created using a top layer above the mask.

During the patterning process, the material of the top layer may affect the properties of the layers underneath the top layer and the mask. Some conventional top layers are made of oxide material. In some cases, an oxide top layer affects the layers underneath the top layer and the mask. Thus, in some cases, the top layer made of oxide is not suitable.

Summary of the Invention

The present invention provides devices having a masking structure and techniques for forming the masking structure. The masking structure includes a mask and a cap layer. The mask is formed from amorphous carbon including transparent amorphous carbon. The cap layer is formed from non-oxide materials.

Brief Description of the Drawings

FIG. 1 through FIG. 11 show cross-sections of a device during various processing stages according to embodiments of the invention.

FIG. 12 through FIG. 23 show cross-sections of a memory device during various processing stages according to embodiments of the invention.

FIG. 24 shows a system according to an embodiment of the invention.

Detailed Description of the Embodiments

The following description and the drawings illustrate specific embodiments of the invention sufficiently to enable those skilled in the art to practice the invention. Other embodiments may incorporate structural, logical, electrical, process, and other changes. In the drawings, like numerals describe substantially similar components throughout the several views. Examples merely typify possible variations. Portions and features of some embodiments may be included in or substituted for those of others. The scope of the invention encompasses the full ambit of the claims and all available equivalents.

FIG. 1 through FIG. 10 show a device 100 during various processing stages according to embodiments of the invention.

FIG. 1 shows a cross-section of a device 100 including a substrate 110. Substrate 110 may represent a part of a wafer, or may be a wafer itself. The wafer may be a semiconductor wafer such as a silicon wafer. Substrate 110 may also be a structure or a layer formed on a wafer. Substrate 110 may include at least one of a

non-conducting material, a conducting material, and a semiconducting material. Examples of non-conducting materials include oxide (e.g., SiO_2, Al_2O_3), nitride (e.g., Si_3N_4), and glass (borophosphosilicate glass-BPSG). Examples of conducting materials include aluminum, tungsten, other metals, and compound of metals. Examples of semiconducting materials include silicon, and silicon doped with other materials such as boron, phosphorous, and arsenic. In embodiments represented by FIG. 1, substrate 110 includes a semiconductor material.

Substrate 110 has a surface 112 in which alignment marks 114 are formed. Alignment marks 114 serves reference points or coordinates of substrate (wafer) 110. During an alignment process, the alignment marks 114 are used to align or position substrate 110 such that structures and layers on substrate 110 can be accurately aligned with each other or with substrate 110.

FIG. 2 shows device 100 with a device structure 220 formed over substrate 210. Device structure 220 includes multiple layers 222, 224, and 226. Each of these multiple layers may include at least one of a non-conducting material, semiconducting material, and a conducting material. For example, layer 222 may be an oxide layer; layer 224 may be a metal layer or a layer having a compound of metal and silicon; and layer 226 may be a nitride layer. In some embodiments, multiple layers 222, 224, and 226 are arranged in an order different from the order shown in FIG. 2. Multiple layers 222, 224, and 226 are formed by growing or deposition or by other known processes. In some embodiments, one or more of the layers 222, 224, and 226 is omitted from device structure 220. In other embodiments, one or more additional layers similar to layers 222, 224, and 226 are added to device structure 220. Device structure 220 has a thickness T2. In some embodiments, T2 is greater than 40000 Angstroms.

FIG. 3 shows device 100 with a mask (layer) 330 formed over device structure 220. Mask 330 is formed from suitable materials to etch device structure 220 in a subsequent etching process. In embodiments represented by FIG. 2, mask 330 is formed from amorphous carbon. Thus, in FIG. 2, mask 330 is also referred to as amorphous carbon layer 330. Amorphous carbon layer 330 has a thickness T3.

In some embodiments, device structure 220 has a certain thickness such that amorphous carbon layer 330 is formed with an adequate to properly etch device structure 220. T3 can be any thickness. In some embodiments, T3 is at least 4000 Angstroms.

In some embodiments, amorphous carbon layer 330 has a low absorption coefficient such that amorphous carbon layer 330 is transparent in visible light range. The visible light range includes electromagnetic radiation having wavelengths between 400 nanometers and 700 nanometers. In some embodiments, amorphous carbon layer 330 has an absorption coefficient (k) between about 0.8 and 0.001 at a wavelength of 633 nanometers. When amorphous carbon layer 330 is transparent in visible light range, amorphous carbon layer 330 is referred to as a transparent amorphous carbon layer. In some embodiments, the transparent amorphous carbon layer has an absorption coefficient (k) between about 0.15 and 0.001 at a wavelength of 633 nanometers.

Amorphous carbon layer 330 may be formed by deposition process. In some embodiments, amorphous carbon layer 330 is formed by chemical vapor deposition (CVD) process. In other embodiments, amorphous carbon layer 330 is formed by plasma enhanced chemical vapor deposition (PECVD) process. Other known processes can also be used to form amorphous carbon layer 330.

In an exemplary PECVD process to form a transparent amorphous carbon layer such as amorphous carbon 330, a process gas including propylene (C_3H_6) is introduced into a PEVCD chamber at an exemplary flow rate between about 500 sccm (standard cubic centimeters per minute) and about 2000 sccm. An additional gas including helium may be also introduced into the chamber at an exemplary flow rate between about 250 sccm and about 500 sccm. Further, embodiments exist where at least one of the hydrocarbon gases is used as the process gas. Examples of the other hydrocarbon gases include CH_4, C_2H_2, C_2H_4, C_2H_6, and C_3H_8. Helium may also be used in combination with at least one of these hydrocarbon gases.

In the above exemplary process to form the transparent amorphous carbon layer such as amorphous carbon 330, a gas mixture is introduced into the chamber.

In this specification, the gas mixture may be either one gas only or a combination of at least two gases. For example, the gas mixture may be either propylene (C_3H_6) only or a combination of propylene and helium. As another example, the gas mixture may be at least one of the propylene, CH_4, C_2H_2, C_2H_4, C_2H_6, and C_3H_8. As a further example, the gas mixture may be at least one of the propylene, CH_4, C_2H_2, C_2H_4, C_2H_6, and C_3H_8 plus helium.

In the exemplary PECVD process of forming the transparent amorphous carbon layer such as amorphous carbon 330, the temperature in the chamber is set between about 200°C and about 500°C. In some embodiments, the temperature in the chamber is set from about 200°C to below about 300°C. The chamber is subjected to a radio frequency (RF) power and a pressure. In some embodiments, the radio frequency power is set between about 400 Watts and about 1000 Watts, and the pressure is set between about 4 Torr and about 7 Torr.

FIG. 4 shows device 100 after a cap layer 440 is formed over amorphous carbon layer 330. Cap layer 440 includes non-oxide materials. Examples of non-oxide materials include boron carbide (B_xC), boron nitride (BN), silicon carbide (SiC), silicon nitride (Si_xN_y), fluorine doped with oxide (e.g., SiO_x:F), fluorine doped with nitride (e.g., Si_xN_y:F), fluorine doped with carbide (e.g., SC:F), and fluoride films such as CaF_x and MgF_x. An example of oxide material includes silicon oxide (SiO_2). In some embodiments, hydrogen is incorporated into the non-oxide materials of cap layer 440. In this specification, fluorinated oxide SiO_x:F is considered as a non-oxide material.

In the examples above, x and y represent the number of atoms in a stable compound. For example, in Si_xN_y, x represents a number of atoms of silicon that form a stable compound with y atoms of nitrogen. In this example, x may be three and y may be four.

Cap layer 440 can be formed by a deposition process such as a CVD and PECVD process. In some embodiments, cap layer 440 is formed together with amorphous carbon layer 330 in the same process (same processing step) such that

cap layer 440 is situ deposited over amorphous carbon layer 330. For example, during or after layer 330 is formed in a CVD or PECVD process similar to the process of described in FIG. 4, a gas including boron such as B_2H_6, B_4H_{10}, and BH_3CO may be introduced to the chamber to form a cap layer 440 having boron carbide over the amorphous carbon layer 330. In some embodiments, cap layer 440 includes boron carbide with about 0.5 atomic percent to about 70 atomic percent of boron.

FIG. 5 shows device 100 after a photoresist layer 550 is formed over cap layer 440. Photoresist layer 550 can be formed by known process. The combination of amorphous carbon layer 330, cap layer 440, and photoresist layer 550 forms a masking structure 560. In some embodiments, masking structure 560 includes an additional layer formed between cap layer 440 and photoresist layer 550; the additional layer serves as an antireflective layer to enhance the photo processing performance. Masking structure 560 is used as a mask to etch one or more layers underneath masking structure 560 in subsequent processes.

FIG. 6 shows device 100 after photoresist layer 550 is patterned. Patterning photoresist layer 550 can be performed using known techniques. The patterned photoresist layer 550 has openings 601.

FIG. 7 shows device 100 after cap layer 440 is patterned. In some embodiments, an oxygen plasma etch process is performed to pattern cap layer 440 using photoresist layer 550 as a mask. After cap layer 440 is patterned, the patterned cap layer 440 has openings 701 continuous or aligned with openings of the patterned photoresist layer 550. FIG. 7 shows patterned photoresist still remains after cap layer 440 is patterned. In some embodiments, however, patterned photoresist layer 550 is removed such that within masking structure 560, only patterned cap layer 440 and amorphous carbon layer 330 remain.

FIG. 8 shows device 100 after amorphous carbon layer 330 is patterned. In some embodiments, amorphous carbon layer 330 is patterned in an etching process such as an oxygen plasma etching process using the patterned cap layer 440 as a

mask. The patterned amorphous carbon layer 330 has openings 801 continuous or aligned with openings 801 of the patterned cap layer 440.

FIG. 9 shows device 100 after photoresist layer 550 is removed. The combination of the remaining cap layer 440 and amorphous carbon layer 330 is used as a mask to etch a portion of device structure 220, or the entire device structure 220, or the entire device structure 220 and at least a portion of substrate 210. In some embodiments, both photoresist layer 550 and cap layer 440 are removed after amorphous carbon layer 330 is patterned. Thus, only amorphous carbon layer 330 remains and is used as a mask to etch the layers underneath amorphous carbon layer 330.

FIG. 10 shows device 100 after device structure 220 is etched. Device structure 220 is etched using cap layer 440 and amorphous carbon layer 330 as a mask. Trenches 1001 are formed as a result of the etching process. In embodiments represented by FIG. 8, trenches 1001 are formed in at least portion of device structure 220. In some embodiments, trenches 1001 are formed in the entire device structure 220 and in at least a portion of substrate 210.

Layer 222 is etched to a level 1002. Level 802 is any level that is above surface 112 of substrate 210. In embodiments represented by FIG. 8, device structure 220 is etched such that the etching process penetrates through layers 226 and 224 and partially into layer 222 and stops at level 1002 as shown in FIG. 8. However, in some embodiments, device structure 220 is etched such that level 802 can be anywhere in device structure 220. In other embodiments, the etching process penetrates through all layers 222, 224, and 226 and stops at or below surface 112 of substrate 210. The level at which the etching process etches into device structure 220 depends on what will be formed after device structure 220 is etched. For example, device structure is etched to one level if conductive interconnects will be formed and at another level if a component such as a capacitor will be formed.

FIG. 11 shows device 100 after cap layer 440 and amorphous carbon layer 330 are removed. Cap layer 440 can be removed by a process such as an oxygen plasma process. Amorphous carbon layer 330 can be removed by a process such as

an ash process. In some embodiments, amorphous carbon layer 330 is removed using an ash process with oxygen plasma or with a combination of oxygen plasma and CF_4.

In the above description of FIG. 3 through FIG. 11, amorphous carbon layer 330, which is transparent in visible light range, is included in masking structure 560 to use as a mask to etch device structure 220. In some embodiments, an amorphous carbon layer such as amorphous carbon layer 330 is also included in device structure 220. For example, one of the layers 222, 224, and 226 of device structure 220 may be an amorphous carbon layer such as amorphous carbon layer 330. As another example, device structure 220 may include an additional layer besides layer 222, 224, and 226 in which the additional layer is an amorphous carbon layer such as amorphous carbon layer 330.

In embodiments where an amorphous carbon layer exists within device structure 220, the amorphous carbon layer within device structure 220 may be used for insulating purposes, antireflection purposes, or for other purposes. Hence, in embodiments where device structure 220 includes an amorphous carbon layer similar to amorphous carbon layer 330, the amorphous carbon layer of device structure 220 still remains after amorphous carbon layer 330 of masking structure 560 is removed.

After amorphous carbon layer 330 is removed as shown in FIG. 10, other processes can be performed to device 100 to form components such as transistors, capacitors, memory cell, or an integrated circuit such as a memory device, a processor, an application specific integrated circuit, or other types of integrated circuits.

In the description of FIG. 1-FIG. 11, device structure 220 may include multiple layers of different materials with different properties. Thus, for different materials in device structure 220, a different masking structure with different materials may be needed to etch device structure 220 such that the materials in the device structure are not affected by the etching process.

In the description above of FIG. 1-FIG. 11, masking structure 560 includes amorphous carbon layer 330 and cap layer 440 in which the cap layer 440 can be formed from different materials such as the non-oxide materials. Since amorphous carbon layer 330 is formed form amorphous carbon, it has a relatively high resistance. Thus, amorphous carbon layer provides a suitable etch selectivity to multiple layers of dielectric material and metal material within device structure 220. Since cap layer 440 may be formed from different types of non-oxide materials, cap layer 440 can be formed with different materials to suit different materials of device structure 220. Thus, the combination of amorphous carbon layer 330 and the different materials of cap layer 440 allows masking structure 560 to be a suitable mask to selectively etch different materials of a device structure such as device structure 220.

Further, when cap layer 440 is in situ deposited together with amorphous carbon layer 330, time and cost may be reduced. In addition, the recipe for forming amorphous carbon layer 330, or cap layer 440, or both may adjusted (selected) to affect the optical property of one or both layers 230 and 440 to improve the reading of the alignment marks on substrate 210. For example, the recipe for amorphous carbon layer 330 or cap layer 440 or both may selected such that one or both of these layers has a low absorption of light to improve the reading of alignment marks such as alignment marks 114 on substrate 210.

FIG. 12 through FIG. 23 show cross-sections of a memory device 1200 during various processing stages according to embodiments of the invention. In FIG. 12, memory device 1200 includes a substrate 1202 having alignment marks 1204 formed on surface 1207 of substrate 1202. A number of surface structures (gate structures) 1205 (1205.1 through 1205.4) are formed over substrate 1202. Within substrate 1202, a number of diffusion regions 1206 (1206.1 through 1206.3) and isolation structures 1207.1 and 1207.2 are formed. For clarity, FIG. 12 shows alignment marks 1204 without elements formed above alignment marks 1204. However, elements such as the layers shown in FIG. 12 may be formed over alignment marks 1204.

Memory device 1200 also includes an insulating layer 1230 and a number of contacts 1240 (1240.1 through 1240.3) extending through insulating layer 1230. Each of the contacts 1240 connects to one of the diffusion regions 1206. A barrier layer 1245 separates surface structures 1205 from insulating layer 1230 and contacts 1240. Contacts 1240 are made of conducting material to provide electrical connections for diffusion regions 1206. Barrier layer 1245 can be oxide, or nitrite, or other non-conducting materials to prevent cross-diffusion of materials between surface structures 1205 and insulating layer 1230. In some embodiments, barrier layer 1245 is omitted. Insulating layer 1230 provides insulation between the contacts 1240. Insulating layer 1230 can be a layer of silicate glass doped with one or more dopants such as boron and phosphorous or other types of doped glasses. For example, insulating layer 1230 can be Boronsilicate glass (BSG), or Phosphosilicate glass (PSG). In embodiments represented by FIG. 12, insulating layer 1230 includes Borophosphosilicate glass (BPSG) and has a thickness T12. In some embodiments, T12 is in the range of 2000 Angstroms to 5000 Angstroms.

In embodiments represented by FIG. 12, substrate 1202 includes silicon doped with a dopant, for example boron, to make it a P-type material. Diffusion regions 1206 are doped with a dopant, for example phosphorous, to make them an N-type material. In some embodiments, substrate 1202 can be an N-type material and diffusion regions 1206 can be a P-type material.

Each of the gate structures 1205 includes a number of elements: a gate dielectric (gate oxide) 1209, a doped polysilicon layer 1212, a silicide layer 1214, a capping dielectric layer 1216, and dielectric spacers 1218. Silicide layer 1214 can include a compound of metal and silicon such as titanium silicide, tungsten silicide, and others. All dielectrics in gate structures 1205 can include material such as silicon oxide. Each of the gate structures 1205 is also referred to as a word line. The structure of FIG. 12 can be formed using known techniques.

FIG. 13 shows memory device 1200 after an insulating layer 1310 is formed. Insulating layer 1310 can include BSG, PSG, or BPSG similar to insulating layer 1230. Insulating layer 1310 and other structures in FIG. 12 form a device structure

1320. Device structure 1320 has a thickness T13. In some embodiments, T13 is at least 40000 Angstroms.

FIG. 14 shows memory device 1200 after a mask 1430 is formed over device structure 1320. Mask 1430 may include amorphous carbon. Thus, mask 1430 is also referred to as amorphous carbon layer 1430. In some embodiments, amorphous carbon layer 1430 has a low absorption coefficient such that amorphous carbon layer 1430 is transparent in visible light range. In some embodiments, amorphous carbon layer 1430 has an absorption coefficient (k) between about 0.8 and 0.001 at a wavelength of 633 nanometers. In other embodiments, amorphous carbon layer 1430 is a transparent amorphous carbon layer in which the transparent amorphous carbon layer has an absorption coefficient (k) between about 0.15 and 0.001 at a wavelength of 633 nanometers. Amorphous carbon layer 1430 may be formed by a method similar to method of forming amorphous carbon layer 330 described in FIG. 4.

Since amorphous carbon layer 1430 is transparent in visible light range, amorphous carbon layer 1430 may be formed at a selected thickness to properly etch device structure 1320 without substantially affecting the reading of the alignment marks 1204 during an alignment of device 1200. Amorphous carbon layer 1430 has a thickness T14, which can be selected at an appropriate value to properly etch device structure 1320. T14 can be any thickness. In some embodiments, T14 is at least 4000 Angstroms.

FIG. 15 shows memory device 1200 after a cap layer 1540 is formed over amorphous carbon layer 1430. Cap layer 1540 includes non-oxide materials such as boron carbide (B_xC), boron nitride (BN), silicon carbide (SiC), silicon nitride (Si_xN_y), fluorine doped with oxide (e.g., SiO_x:F), fluorine doped with nitride (e.g., Si_xN_y:F), fluorine doped with carbide (e.g., SC:F), and fluoride films such as CaF_x and MgF_x. In some embodiments, hydrogen is incorporated into the non-oxide materials of cap layer 1540. Cap layer 1540 can be formed by a process such as CVD or PECVD process. In some embodiments, cap layer 1540 is formed together

with amorphous carbon layer 1430 in the same process (same processing step) such that cap layer 1540 is situ deposited over amorphous carbon layer 1430. For example, during or after amorphous carbon layer 1430 is formed in a CVD or PECVD process similar to the process of described in FIG. 4, a gas including boron such as B_2H_6, B_4H_{10}, and BH_3CO can be introduce to the chamber to form cap layer 1540 having boron carbide over the amorphous carbon layer 1430. In some embodiments, cap layer 1540 includes boron carbide with about 0.5 atomic percent to about 70 atomic percent of boron.

FIG. 16 shows device 1200 after a photoresist layer 1650 is formed over cap layer 1540. Photoresist layer 1650 can be formed by a known process. The combination of amorphous carbon layer 1430, cap layer 1540, and photoresist layer 1650 forms a masking structure 1660. In some embodiments, masking structure 1540 includes an additional layer formed between cap layer 1540 and photoresist layer 1650; the additional layer serves as an antireflective layer to enhance the photo processing performance. Masking structure 1660 is used as mask to etch one or more layers underneath masking structure 1660 in subsequent processes.

FIG. 17 shows device 1200 after photoresist layer 1650 is patterned. Patterning photoresist layer 1650 can be performed using known techniques. The pattern photoresist layer 1650 has openings 1701.

FIG. 18 shows device 1200 after cap layer 1540 is patterned. In some embodiments, cap layer 1540 is patterned in an etching process such as an oxygen plasma etching process using photoresist layer 1650 as a mask. After cap layer 1540 is patterned, the patterned cap layer 1540 has openings 1801 continuous or aligned with openings of the patterned photoresist layer 1650. FIG. 17, shows patterned photoresist still remains after cap layer 1540 is patterned. In some embodiments, however, patterned photoresist layer 1650 is such that within masking structure 1660, only patterned cap layer 1540 and amorphous carbon layer 1430 remain.

FIG. 19 shows device 1200 after amorphous carbon layer 1430 is patterned. In some embodiments, amorphous carbon layer 1430 is patterned in an etching

process such as an oxygen plasma etching process using the patterned cap layer 1540 as a mask. The patterned amorphous carbon layer 1430 has openings 1901 continuous or aligned with openings of the patterned cap layer 1540.

FIG. 20 shows device 1200 after photoresist layer 1650 is removed. The combination of the remaining cap layer 1340 and amorphous carbon layer 1430 is used as a mask to etch a portion of device structure 1320, or the entire device structure 1320, or the entire device structure 1320 and at least a portion of substrate 1202. In some embodiments, both photoresist layer 1650 and cap layer 1540 are removed after amorphous carbon layer 1430 is patterned. Thus, only amorphous carbon layer 1430 remains and is used as a mask to etch the layers underneath amorphous carbon layer 1430.

FIG. 21 shows device 1200 after device structure 1320 is etched. Device structure 1320 is etched using cap layer 1540 and amorphous carbon layer 1430 as a mask. The etched device structure 1320 has openings 2101.

FIG. 22 shows device 1200 after cap layer 1540 and amorphous carbon layer 1430 are removed. The process of removing cap layer 1540 and amorphous carbon layer 1430 is similar to that of cap layer 440 and amorphous carbon layer 330 of FIG. 11.

FIG. 23 shows device 1200 after other layers are formed using known techniques. In each of the openings 2101, a first conductive layer 2302 (2302.1 and 2302.2), a second conductive layer 2304 (2304.1 and 2304.2), and a dielectric layer 2306 (2306.1 and 2306.2) are formed. Conductive layers 2302, 2304, dielectric layer 2306 and other elements form storage capacitors C1 and C2. For example, in storage capacitor C1, conductive layer 2302.1, contact 1240.1, and diffusion region 1206.1 form a first capacitor plate (bottom plate); conductive layer 2302.2 forms a second capacitor plate (top plate); and dielectric layer 2306.1 is the capacitor dielectric. In some embodiments, conductive layers 2304 connect to common a cell plate of memory device 1200. The common cell plate is omitted from FIG. 19 for simplicity.

Memory device 1200 includes access transistors T1 and T2. Gate structure 1205.2 and diffusion regions 1206.1-1206.2 form access transistor T1. Gate structure 1205.3 and diffusion regions 1206.2-1206.3 form access transistor T2. Access transistor T1 and storage capacitor C1 form a memory CELL1. Access transistor T2 and storage capacitor C2 form a memory CELL2.

Memory cells CELL1 and CELL2 store data in form of charge in storage capacitors C1 and C2. The charges are transferred to and from doped regions 1206.1 and 1206.3 of capacitors C1 and C2 via contact 1240.2. In some embodiments, contact 1240.2 is a buried bit line contact, which connects to a bit line of memory device 1200.

In other embodiments, other elements having structures different from the structures of the layers 2302, 2304, and 2306 can be formed in openings 2101 (FIG. 21). For example, interconnects instead of capacitor plates can be formed in openings 2101 to connect diffusion regions 1206 to other parts of memory device 1200.

Memory device 1200 may be a dynamic random access memory (DRAM) device. Examples of DRAM devices include synchronous DRAM commonly referred to as SDRAM, SDRAM II, SGRAM (Synchronous Graphics Random Access Memory), DDR SDRAM (Double Data Rate SDRAM), DDR II SDRAM, DDR III SDRAM, GDDR III SDRAM (Graphic Double Data Rate), and Rambus DRAMs. Memory device 1200 includes other elements, which are not shown for clarity.

FIG. 24 shows a system according to an embodiment of the invention. System 2400 includes a chamber 2410 and a wafer 2420 placed in the chamber. In some embodiments, chamber 2410 is a PECVD chamber and wafer 2420 is a semiconductor wafer. An example of chamber 2410 includes a chamber of the Producer Processor available from Applied Materials, Inc. located in Santa Clara, California. Chamber 2410 and wafer 2420 can be used to form part of device 100 (FIG. 1-FIG. 11) and memory device 1200 (FIG. 12-23).

Wafer 2420 includes a number of alignment marks 2414 and a number of dice 2430. In some embodiments, alignment marks 2414 represent alignment marks 114 (FIG. 1) and alignment marks 1204 (FIG. 12).

At least one of the dice 2430 includes elements according to embodiments described in FIG. 2-FIG. 23 above. For example, at least one of the dice 2430 includes a substrate, a device structure, and a masking structure such as that of devices 100 and 1200 (FIG. 2-FIG. 23). Thus, at least one of the dice 2430 includes an amorphous carbon layer such as amorphous carbon layer 330 (FIG. 4) and amorphous carbon layer 1430 (FIG. 13) formed according to the process described in FIG. 2-FIG. 23.

A die such as one of the dice 2430 is a pattern on a semiconductor wafer such as wafer 2420. A die contains circuitry to perform a specific function. For, example, at least one of the dice 2430 contains circuitry for a device such as a processor, or memory device such as memory device 1200 (FIG. 11-FIG. 23).

Conclusion

Various embodiments of the invention provide a device having a masking structure and a method for forming the device. The masking structure includes an amorphous carbon layer on a cap layer. The amorphous carbon layer may be a transparent amorphous carbon layer. The cap layer includes non-oxide materials. Although specific embodiments are described herein, those skilled in the art recognize that other embodiments may be substituted for the specific embodiments shown to achieve the same purpose. This application covers any adaptations or variations of the present invention. Therefore, the present invention is limited only by the claims and all available equivalents.